Electronic Version
Stylesheet Version v1.1.1

METHOD OF PERFORMING DESIGN RULE CHECKING

Abstract

A method of performing latch up check on an integrated circuit (IC) design that comprises rasterizing a conductor region shape and contact shapes and iteratively expanding the contact shapes within the conductor region shape using a cellular algorithm. Direction values for contact cells can be used to limit the number of neighboring cells which must be explored. In every fourth iteration of the expansion process, corner cells may not be expanded. Reachable areas outside of conductors can also be explored.